REMARKS

In the Office Action, the examiner objected to the claims because of the informalities involved in Claim 1, 17 and 22. Accordingly, the applicant has amended the claims to correct the informalities. In this opportunity, the applicant has corrected minor wording problems in the claims.

The Examiner rejected Claims 1, 2, 6, 7, 17 and 18 under 35 U.S.C. 102(e) as being anticipated by Gutnik et al. (U.S. Patent No. 6,661,860). The Examiner rejected Claims 3, 5, 8, 19 and 21-24 under 35 U.S.C. 103(a) as being unpatentable over Gutnik et al. (U.S. Patent No. 6,661,860) in view of Dala et al. (U.S. Patent No. 6,661,836). The Examiner rejected Claims 4 and 20 under 35 U.S.C. 103(a) as being unpatentable over Gutnik et al. (U.S. Patent No. 6,661,860) in view of Voorakaranam et al. (Proceedings of 43rd IEEE Midwest Symposium on Circuits and Systems). The Examiner rejected Claims 13, 14 and 32 under 35 U.S.C. 103(a) as being unpatentable over Gutnik et al. (U.S. Patent No. 6,661,860) in view of Godard (U.S. Patent No. 4,654,861).

Accordingly, the applicant has amended Claims 1 and 17 to more clearly distinguish the features of the present invention from the technologies disclosed by the cited references. More specifically, the applicant has added the new limitation "wherein said generation probability of the peak-to-peak value is estimated without actually measuring the peak-to-peak values of the clock signals under test" to Claim 1. Similarly, the applicant has added the new limitation

"wherein said generation probability of the peak-to-peak value is estimated without actually measuring the peak-to-peak values of the clock signals under test" to Claim 17.

One of the essential features of the present invention resides in the fact that the probability estimating apparatus and method of the present invention estimates the peak-to-peak values in clock skews among a plurality of clock signals under test without actually measuring the peak-to-peak values of the clock signals. This determination is made based on the estimation calculated with use of a predetermined scattering property, such as, but not limited to, Rayleigh scattering. For example, at page 23, lines 13-29, such an essential feature of the present invention is described with reference to Figure 14, as follows:

> In Figure 14, the samples and peak-to-peak values are plotted for the clock skews between the two signals under test, which have been distributed within the microprocessor. The upper diagram shows the test results in the quiet mode in the microprocessor, and the lower diagram shows the test results in the noise mode. The theoretical curve in the diagrams are calculated from the inverse probability $P_r(Z_{pp}>Z_{pp})$ expressed by the equation (38). The test data complies very well with the theoretical curves of the Rayleigh distribution (especially in the noise mode).

Namely, with use of the equation 38, the present invention estimates the peak-to-peak values in the clock skews among the clock signals under test without actually measuring the peak-to-peak values of the clock signals. Figure 14 shows the correctness of the estimated results of the generation probability of the peak-to-peak value in the present invention by comparing with the

actually measured results. In Figure 14, the estimated results are represented by the solid lines and the measured results are represented by the small circles.

The cited Gutnik et al. reference discloses, as shown in Figure 1, a digital circuit which includes a plurality of arbiters, each arbiter having first and second input ports and an output port providing an output signal. Each first input of the plurality of arbiters is connected to a first common line and each second input of the plurality of arbiters is connected to a second common line. The output signal of each arbiter will transition to a first state if a first input signal is high and a second input signal is low. The digital circuit further includes a decision circuit, having a plurality of inputs and an output. Each of the inputs of the decision circuit is connected to a corresponding output of one of the plurality of arbiters. The decision circuit output provides a signal indicative of the time difference between a signal fed to the first common line and a signal fed to the second common line.

In the cited Gutnik et al. reference, with such an arrangement noted above, the difference in arrival times can be measured between digital signal edges of two pulses. Based on the difference between the minimum value and the maximum value of the arrival times, the digital circuit obtains the peak-to-peak value of the signals supplied to the common lines. In other words, the digital circuit in the cited Gutnik et al. reference has to

actually measure the peak-to-peak values by measuring the minimum value (one peak) and the maximum value (another peak). This is more clearly evidenced by the descriptions at column 6, lines 43-60 which reads as follows:

> As the pulse transitions form a low to a high, the center of the slope is typically referred to as the crossover point. Consider an arbiter to which two signals are repeatably applied. A perfectly balanced arbiter would output a 1 in half of the trials and a 0 in the other half of the trials when inputs to the arbiter are exactly simultaneous. If one input is leading, the fraction of the trials in which the arbiter outputs a 1 goes up. If the other input is leading, the fraction of the trials in which the arbiter outputs a 0 goes up. The "crossover point," where probability of a 1 output equals the probability of a 0 output, can be said to be at 0 offset in this case. A real arbiter would have some imbalance. For example, when the inputs are simultaneous, it might output a 1 in 2/3 of the trials, and a 0 in the other 1/3 of the trials. It might output a 1 in half the trials and a 0 in the other half of the trials if the one input signal is 10 picoseconds later than the other. In that case, the arbiter may be said to have a crossover point of 10 picoseconds. (If the signals were reversed, it would have a crossover point of -10 picoseconds).

As described in the extract, based on the probability of logic 1 and logic 0 from the outputs of the arbiters which are assigned with predetermined crossover times, the digital circuit obtains the jitter (time difference between two edges) of the signals under test. Further, in the cited Gutnik et al. reference, as described at column 10, lines 25-38, the peak-to-peak jitter is obtained by the difference between the minimum and maximum measured time differences (jitter), which reads as follows:

> Jitter is the temporal variation in time difference between two edges. Jitter at a single node may be determined by iteratively comparing the difference between the edges of the clock at that node and the clock

> supplied by a reference clock. More generally, the jitter between any two clocks, either both in the system under test or one in the system under test and one external reference, may be computed by repeatedly measuring the time difference between rising edges of the two clocks, and tabulating the results. The peak-to-peak jitter is the difference between the minimum and maximum measured time differences. Thus, the information provided by the output signals of the arbiters are utilized to characterize the jitter of a circuit from which the clock signal originated.

In the present invention, however, the probability estimating apparatus and method estimates the generation probability of the peak-to-peak values without actually measuring the peak-to-peak values (time differences between the edges) of the clock signals as noted above. Thus, the principle of operation is fundamentally different from that of the cited Gutnik et al. reference. The applicant has clarified this difference by the amendment made in Claims 1 and 17. Therefore, the applicant believes that the rejection under 35 U.S.C. 102(e) is no longer applicable to the present invention. As discussed above, the present invention is fully distinguishable from the cited Gutnik et al. reference, and this reference is used in the rejection under 35 U.S.C. 103(a) in combination with other references. Therefore, the applicant believes that the rejection under 35 U.S.C. 103(a) is no longer applicable to the present invention as well.

The applicant has added new Claims 34-37. Basically, independent Claim 34 is a combination of original Claims 1 and 7, and independent Claim 36 is a combination of original Claims 17 and

23. Claim 35 corresponds to original Claim 5 and Claim 37 corresponds to original Claim 21.

In the office action, the examiner rejected Claim 7 which includes the feature of "frequency multiplier" on the ground the that the cited Gutnik et al. reference discloses the frequency multiplier at column 6, lines 11-21. The applicant respectfully disagrees with the examiner regarding the interpretation of the technology disclosed by the this cited reference. What is disclosed by Gutnik et al. at column 6, line 11-21 is as follows:

> By using multiple arbiters, you are averaging over multiple arbiters to get linearity and average noise. With this technique, it is possible to keep improving accuracy and precision simply by adding more arbiters to the arbiter array 28 as described above. As described below, an algorithm to measure the r vs. dT curve for a particular array is useful, so that r, which is a digital output, can be converted to dT. Results indicate that resolution on the order of greater than 2 picoseconds are possible.

Nowhere in this description is it stated that the jitter estimation system includes a frequency multiplier. In the cited Gutnik et al. reference, a plurality of arbiters are provided in parallel so that the input signals are commonly connected to the plural arbiters. The output of all of the arbiters are connected to the decision logic circuit. The arbiters are arranged to have slightly different crossover time from one another. Thus, depending on the timing of the input signals, some of the arbiters produce logic "1" at the outputs while other arbiters produce logic "0" at the outputs. The decision logic circuit determines the

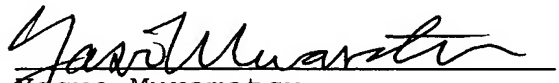
jitter based on which fraction of arbiters indicate the logic "1" and which fraction of the arbiters indicate the logic "0".

In this arrangement, it is apparent that the measurement accuracy will increase by increasing the number of arbiters. The description quoted above states that the accuracy and precision can be improved by simply adding more arbiters. This feature of the cited Gutnik reference is unrelated to the frequency multiplier of the present invention. It should be noted that the use of multiple arbiters in the cited Gutnik et al. reference does not mean that the frequency of the clock signal is multiplied. The idea of multiplying the clock frequency is not shown or suggested anywhere in the cited Gutnik et al. reference. Therefore, the invention defined in Claims 34-37 are patentable over the prior art.

In view of the foregoing, the applicant believes that Claims 1-37 are in condition for allowance, and the applicant respectfully requests that the application be allowed and passed to issue.

Respectfully submitted,

MURAMATSU & ASSOCIATES

Dated: 11/14/05 By: 

Yasuo Muramatsu
Registration No. 38,684
Attorney of Record
114 Pacifica, Suite 310
Irvine, CA 92618
(949) 753-1127

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